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Design and Analysis of Multi Level D-STATCOM to Improve the Power Quality

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Abstract
In the last decade, the electrical power quality issue has been the main concern of the power companies. Power quality is defined as the index which both the delivery and consumption of electric power affect on the performance of electrical apparatus. From a customer point of view, a power quality problem can be defined as any problem is manifested on voltage, current, or frequency deviation that results in power failure. The power electronics progressive, especially in flexible alternating-current transmission system (FACTS) and custom power devices, affects power quality improvement. This paper presents an investigation of seven-Level Cascaded H - bridge (CHB) Inverter as Distribution Static Compensator (DSTATCOM) in Power System (PS) for compensation of reactive power and harmonics. The advantages of CHB inverter are low harmonic distortion, reduced number of switches and suppression of switching losses. The DSTATCOM helps to improve the power factor and eliminate the Total Harmonics Distortion (THD) drawn from a Non-Liner Diode Rectifier Load (NLDRL). The D-Q reference frame theory is used to generate the reference compensating currents for DSTATCOM while Proportional and Integral (PI) control is used for capacitor dc voltage regulation. A CHB Inverter is considered for shunt compensation of a 11 Kv distribution system. Finally a level shifted PWM (LSPWM) and phase shifted PWM (PSPWM) techniques are adopted to investigate the performance of CHB Inverter. The results are obtained through Matlab/Simulink software package.

Keywords — FACTS, DSTATCOM, Cascaded H - bridge (CHB) Inverter, Total Harmonics Distortion (THD).

I. Introduction

A DSTATCOM is a device which is used in an AC distribution system where, harmonic current mitigation, reactive current compensation and load balancing are necessary. The building block of a DSTATCOM is a voltage source converter (VSC) consisting of self commutating semiconductor valves and a capacitor on the DC bus.

The device is shunt connected to the power distribution network through a coupling inductance that is usually realized by the transformer leakage reactance. In general, the DSTATCOM can provide power factor correction, harmonics compensation and load balancing. The major advantages of DSTATCOM compared with a conventional static VAR compensator (SVC) include the ability to generate the rated current at virtually any network voltage, better dynamic response and the use of a relatively small capacitor on the DC bus.

Fig. 1 shows the schematic diagram of a DSTATCOM connected to a three phase AC mains feeding three phase loads. Three phase loads may be a lagging power factor load or an unbalanced load or non-linear loads or mixed of these loads. For reducing ripple in compensating currents, interfacing inductors (Lf) are used at AC side of the voltage source converter (VSC). A small series connected capacitor (Cf) and resistor (Rf) represent the ripple filter installed at PCC in parallel with the loads and the compensator to filter the high frequency switching noise of the voltage at PCC.

The STATCOM used in distribution systems is called DSTACOM (Distribution-STACOM) and its configuration is the same, but with small modifications. It can exchange both active and reactive power with the distribution system by varying the amplitude and phase angle of the converter voltage with respect to the line terminal voltage. A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. There are several types of multilevel inverters: cascaded R-bridge (CRB), neutral point clamped, flying capacitor [2-5]. In particular, among these topologies, CRB inverters are being widely used because of their modularity and simplicity.

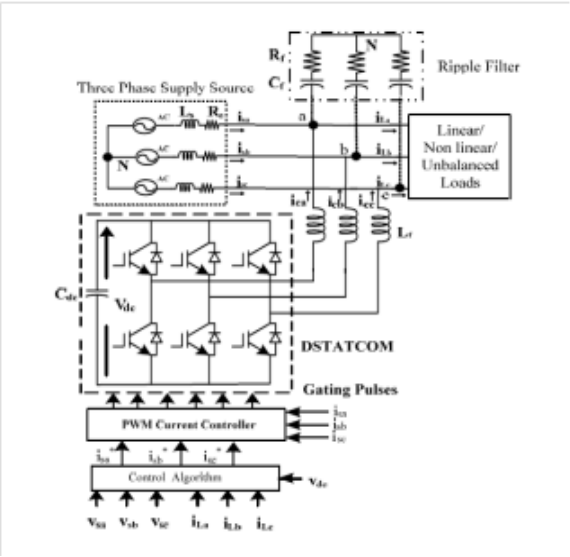

Fig.1 Schematic diagram of D-STATCOM

Various modulation methods can be applied to CRB inverters. CRB inverters can also increase the number of output voltage levels easily by increasing the number of R-bridges. This paper presents a DSTATCOM with a proportional integral controller based CRB multilevel inverter for the harmonics and reactive power mitigation of the nonlinear loads. This type of arrangements have been widely used for PQ applications due to increase in the number of voltage levels, low switching losses, low electromagnetic compatibility for hybrid filters and higher order harmonic elimination.

II. DESIGN OF MULTILEVEL BASED DSTATCOM

A. Principle of DSTATCOM

AD-STATCOM (Distribution Static Compensator), which is schematically depicted in Figure- I, consists of a two-level Voltage Source Converter (VSC), a dc energy storage device, a coupling transformer connected in shunt to the distribution network through a coupling transformer.

The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the DSTATCOM and the ac system. Such configuration allows the device to absorb or generate controllable active and reactive power. The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes:

I. Voltage regulation and compensation of reactive power;
2. Correction of power factor
3. Elimination of current harmonics.

Here, such device is employed to provide continuous voltage regulation using an indirectly controlled converter.

As shown in Figure-l the shunt injected current Ish corrects the voltage sag by adjusting the voltage drop across the system impedance Zth. The value of Ish can be controlled by adjusting the output voltage of the converter. The shunt injected current Ish can be written as,

$$I_{sh} = I_L - I_S = I_L - (V_{th} - V_L) / Z_{th} \quad (1)$$

$$I_{sh} /\_\eta = I_L /\_- \theta \quad (2)$$

The complex power injection of the D-STATCOM can be expressed as,

$$S_{sh} = V_L I_{sh}^* \quad (3)$$

It may be mentioned that the effectiveness of the DSTATCOM in correcting voltage sag depends on the value of Zth or fault level of the load bus. When the shunt injected current Ish is kept in quadrature with V L, the desired voltage correction can be achieved without injecting any active power into the system. On the other hand, when the value of Ish is minimized, the same voltage correction can be achieved with minimum apparent power injection into the system. It may be mentioned that the effectiveness of the DSTATCOM in correcting voltage sag depends on the value of Zth or fault level of the load bus. When the shunt injected current Ish is kept in quadrature with V L, the desired voltage correction can be achieved without injecting any active power into the system. On the other hand, when the value of Ish is minimized, the same voltage correction can be achieved with minimum apparent power injection into the system.

B. Control for Reactive Power Compensation

The aim of the control scheme is to maintain constant voltage magnitude at the point where a sensitive load under system disturbances is connected. The control system only measures the rms voltage at the load point, i.e., no reactive power measurements are required. The VSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. Since custom power is a relatively low-power application, PWM methods offer a more flexible option than the fundamental frequency switching methods favored in FACTS applications. Apart from this, high switching frequencies can be used to improve on the efficiency of the converter, without incurring significant switching losses.

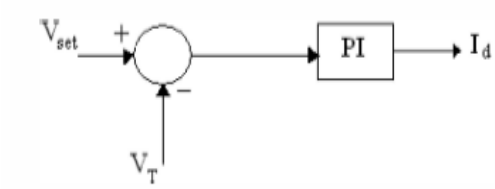

Fig.2 PI Control for reactive power compensation

The controller input is an error signal obtained from the reference voltage and the rms terminal voltage measured. Such error is processed by a PI controller; the output is the angle 0, which is provided to the PWM signal generator. It is important to note that in this case, of indirectly controlled converter, there is active and reactive power exchange with the network simultaneously. The PI controller processes the error signal and generates the req uired angle to drive the error to zero, i.e. the load rms voltage is brought back to the reference voltage.

C. Control for Harmonics Compensation

The Modified Synchronous Frame method is presented in [7]. It is called the instantaneous current component (idiq) method. This is similar to the Synchrous Reference Frame theory (SRF) method. The transformation angle is now obtained with the voltages of the ac network. The major difference is that, due to voltage harmonics and imbalance, the speed of the reference frame is no longer constant. It varies instantaneously depending of the waveform of the 3-phase voltage system. In this method the compensating currents are obtained from the instantaneous active and reactive current components of the nonlinear load. In the same way, the mains voltages V(a,b,c) and the available currents ij (a,b,c) in a- components must be calculated as given by (4), where C is Clarke Transformation Matrix. However, the load current components are derived from a SRF based on the Park transformation, where '8' represents the instantaneous voltage vector angle (5).

$$\begin{bmatrix} I_{l\alpha} \\ I_{l\beta} \end{bmatrix} = [C] \begin{bmatrix} I_{la} \\ I_{lb} \\ I_{lc} \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} I_{ld} \\ I_{lq} \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} I_{l\alpha} \\ I_{l\beta} \end{bmatrix}, \theta = tan^{-1}\frac{V_\beta}{V_\alpha} \quad (5)$$

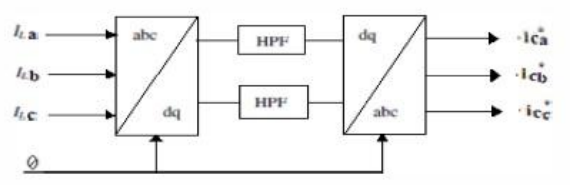

Fig.3 Block diagram of SRF method

Fig. 3 shows the block diagram SRF method. Under balanced and sinusoidal voltage conditions angle fI is a uniformly increasing function of time. This transformation angle is sensitive to voltage harmonics and un balance; therefore dI /d t may not be constant over a mains period. With transformation given below the direct voltage component is

$$\begin{bmatrix} i_{ld} \\ i_{lq} \end{bmatrix} = \frac{1}{\sqrt{V_\alpha^2+V_\beta^2}} \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} = \frac{1}{\sqrt{V_\alpha^2+V_\beta^2}} \begin{bmatrix} V_\alpha & -V_\beta \\ V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} \quad (7)$$

$$\begin{bmatrix} I_{Comp,a} \\ I_{Comp,b} \\ I_{Comp,c} \end{bmatrix} = [C]^T \begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} \quad (8)$$

D. Cascaded H-Bridge Multilevel Inverter:-

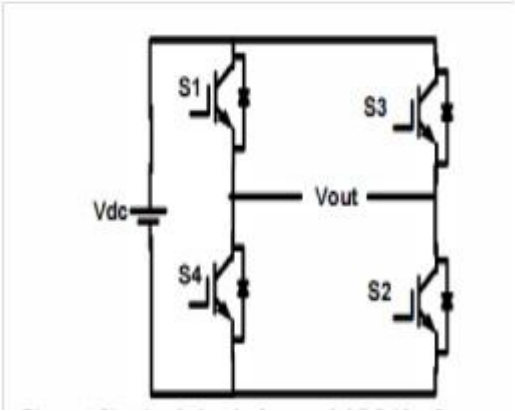

Fig.4 Circuit of the single cascaded H-Bridge Inverter

III. 5 level SIMULINK diagram

PWM Techniques for CHB Inverter

The most popular PWM techniques for CHB inverter are

1. Phase Shifted Carrier PWM (PSCPWM),
2. Level Shifted Carrier PWM (LSCPWM).

1. Phase Shifted Carrier PWM (PSCPWM):

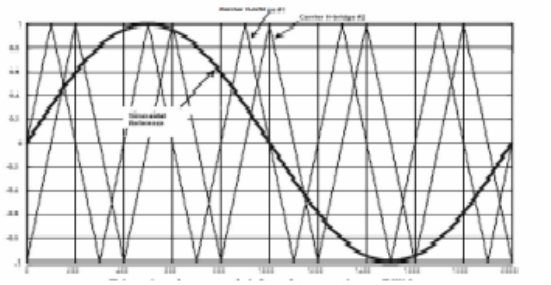

Fig.5 Phase Shifted Carrier PWM

Fig.5 shows the Phase shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal Unipolar pulse width

modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier phase shift of 1800 1m (No. of levels) for cascaded inverter 1S introduced across the cells to generate the stepped multi level output waveform with lower distortion.

2. Level Shifted Carrier PWM (LSCPWM)

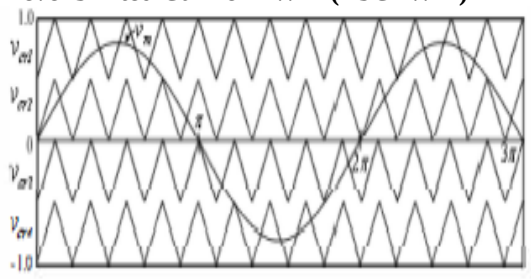

Fig.6 Level Shifted Carrier PWM

Fig.6 shows the Level shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier Level shift by 11m (No. of levels) for cascaded inverter 1S introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

IV. MATLAB/SIMULINK MODELING AND SIMULATION RESULTS

Fig.7 shows the Matab/Simulink power circuit model of DSTATCOM. It consists of five blocks named as source block, non linear load block, control block, APF block and measurements block. The system parameters for simulation study are source voltage of llkv, 50 hz AC supply, DC bus capacitance ISSOe-6 F, Inverter series inductance 10 mH, Source resistance of 0.1 ohm and inductance of 0.9 mHo Load resistance and inductance are chosen as 30mH and 60 ohms respectively.

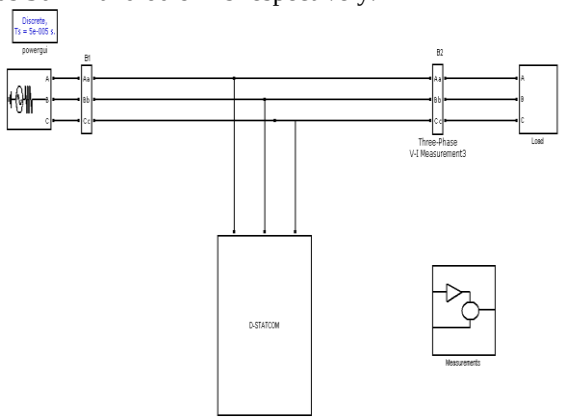

Fig.7 Matab/Simulink power circuit model of DSTATCOM.

V. SIMULATION RESULTS

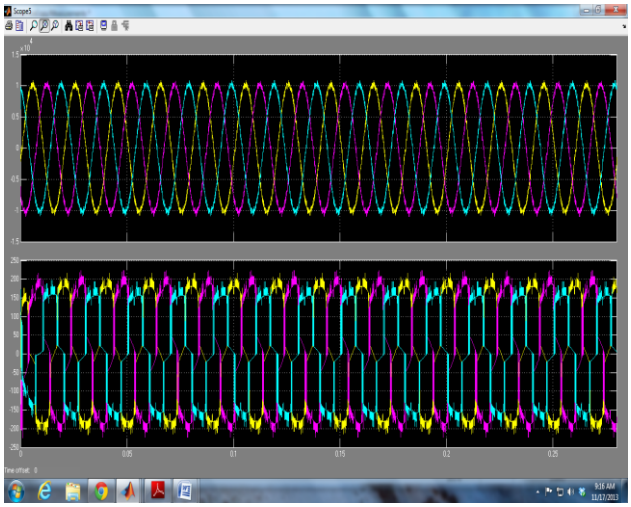

Fig.8 source and load currents with D-STATCOM

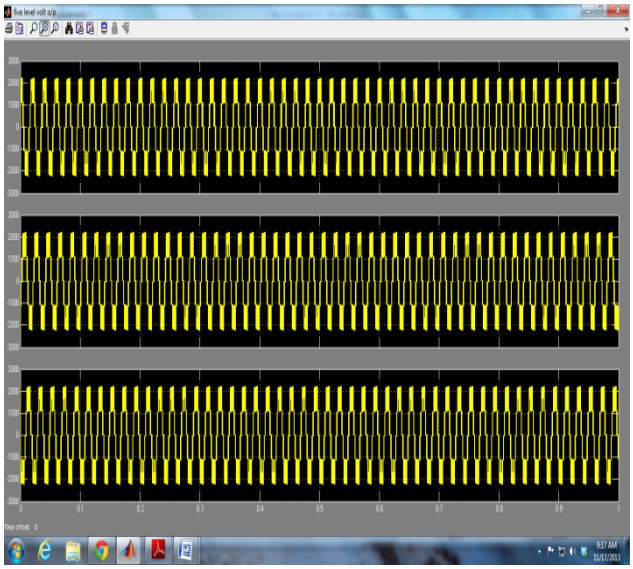

Fig.9 Individual 5 level voltages

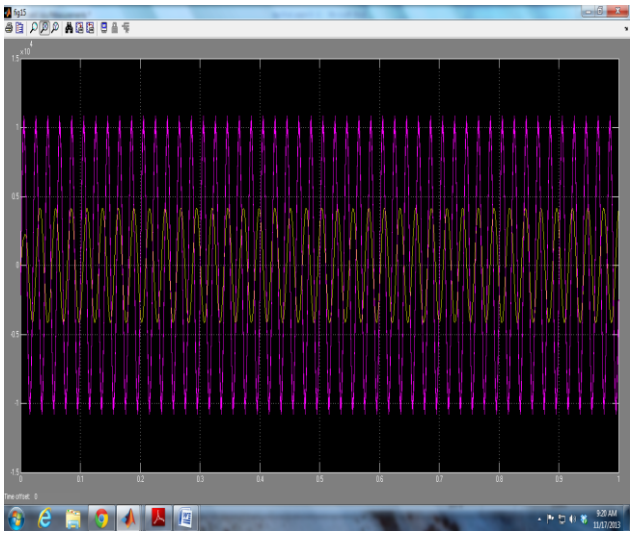

Fig.10 Source voltage and source current

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